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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,200	09/01/2004	Bruce B. Doris	FIS920040152US1	5199

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EXAMINER	
LE, DUNG ANH	
ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
10/30/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
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Office Action Summary	Application No.	Applicant(s)	
	10/711,200	DORIS ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/1/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections

Claim Rejections - 35 USC § 102

Claims 1- 3, 5 and 8- 9 are rejected under 35 USC 102 (e) as being anticipated by Achuthan et al. (7125776 B2).

Achuthan teaches a transistor comprising:

a stack (especially see figs. 1-5 and refer to related texts) comprising:

a silicon on insulator layer 110 having a plurality of channels;

a silicon oxide insulation layer 120 adjacent the silicon on insulator layer ; and

a dielectric layer 130 adjacent the silicon oxide insulation layer 120; and

a gate electrode 320 , wherein the gate electrode 320 covers a portion of the stack; wherein at least one channel has a gate configuration that is different than remaining channels of plurality of channel (especially see figs. 1-5 and refer to related texts).

Regarding claim 2, wherein the at least one channel has a first thickness that is greater than the thickness of the remaining channels (fig. 5 and refer to related texts).

Regarding claim 3, wherein the at least one channel has a different gate dielectric than the remaining channels (fig. 5 and refer to related texts).

Regarding claim 5, wherein the stack further comprises a protection layer 140 located between the dielectric layer 130 and the gate electrode 320 (col 3, lines 15-20 , fig. 3 and refer to related texts).

Regarding claim 8, wherein the dielectric layer 130 is a high-k dielectric material.

Regarding claim 9, wherein the stack and the gate electrode are incorporated into a finFET device (fig. 5 and refer to related texts).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 6-7 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Achuthan et al. in view of the following remark.

Regarding claim 4, Achuthan teaches the claimed invention as applied to claims 1 and 3 except for the gate dielectric of the remaining channels is a material selected from the group comprising silicon dioxide, nitride oxide, and a silicon oxide that has undergone a plasma nitridation process as cited in current claim 4.

However, the process limitation "a silicon oxide that has undergone a plasma nitridation process." is taken to be a product by process limitation and consider non-limitation. In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim 6-7, Achuthan teaches the claimed invention as applied to claims 1 and 5 except for wherein the protection layer is a metal and wherein the protection layer is a thin polysilicon as cited in current claims 6-7.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the protection layer is a metal and wherein the protection layer is a thin polysilicon, the abovementioned material commonly used as a mask or protecting layer to protect underlying layer in a etching or patterning process , since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the desired application.

Set of claims 10-13

Claims 10, 11-12 are rejected under 35 USC 102 (e) as being anticipated by Achuthan et al. (7125776 B2).

Achuthan teaches a transistor (especially see figs. 1-5 and refer to related texts) comprising:

a stack comprising:

a silicon on insulator layer 110;

a silicon oxide insulation layer 120 on the silicon on insulator layer;

a dielectric layer 130 on the silicon oxide insulation layer, wherein the dielectric layer is a high-k dielectric material; and

a protection layer 140 (col 3, lines 15-20) on the dielectric layer; and

a gate electrode 320 covering a portion of the stack.

Regarding claim 13, wherein the stack and the gate electrode are incorporated into a finFET device (fig. 5 and refer to related texts).

Claims 11-12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Achuthan et al. (7125776 B2) in view of the following remark.

Achuthan teaches the claimed invention as applied to claims 10 except for wherein the protection layer is a metal and wherein the protection layer is a thin polysilicon as cited in current claims 11-12.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the protection layer is a metal and wherein the protection layer is a thin polysilicon, the abovementioned material are commonly used as a mask or protecting layer to protect underlying layer in a etching or patterning process , since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the desired application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on (571) 272-1657. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Dung A. Le/

DUNG A. LE
Primary Examiner
Art Unit 2818